UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,485	10/16/2003	Jen Kuang Fang	4459-087A	5378

7590 05/18/2004

LOWE HAUPTMAN GILMAN & BERNER, LLP
Suite 300
1700 Diagonal Road
Alexandria, VA 22314

EXAMINER	
SMOOT, STEPHEN W	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/685,485	FANG, JEN KUANG	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10-16-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 16 October 2003.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method of Forming a Package Assembly that Includes Solder Bump Connecting of a Heat Sink to a Flip Chip.

2. The disclosure is objected to because of the following informality:

Update the first sentence of the specification to indicate that US Patent Application Serial No. 10/118,002 is --now abandoned--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 11, 13-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Ho et al. (US 6,507,104 B2).

Referring to Figs. 3, 4A-4D and column 4, line 4 to column 5, line 26, Ho et al. disclose a semiconductor packaging method that includes the following features:

- A substrate (30) with a plurality of bonding pads (302) and a plurality of ball pads (303);
- A semiconductor chip (31) with a plurality of solder bumps (32) on its active side (310);
- A heat sink (33) with a plurality of solder balls (34) attached to one side (331);
- The heat sink (33) can be made of copper or aluminum;
- The semiconductor chip (31) is positioned on the substrate (30) with the solder bumps (32) aligned with the bonding pads (302);
- The heat sink (33) is placed over the semiconductor chip (31) with the solder balls (34) aligned with the ball pads (303);
- The solder bumps (32) and solder balls (34) are reflowed simultaneously; and

- The remaining space between the substrate (30), the chip (31), and the heat sink (33) is encapsulated with epoxy resin (36) during a molding process, which implies curing of the epoxy resin.

These are all of the limitations set forth in claims 11, 13-14 of the applicant's invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (US 6,437,240 B2 from applicant's IDS) in view of Ho et al. (US 6,507,104 B2).

Referring to Fig. 25 and column 29, line 45 to column 31, line 39, Smith discloses a semiconductor packaging method that includes the following features:

- A flexible dielectric sheet (1512) with a plurality of contacts (1519) formed on one side;
- A semiconductor chip (1524a) with a plurality of solder bumps (1550a) on its active side;
- A heat sink (1542) with a plurality of solder bumps (1550b) attached to one side;

- The heat sink (1542) can be made of aluminum;
- The semiconductor chip (1524a) is positioned on the dielectric sheet (1512) with the solder bumps (1550b) aligned with the contacts (1519);
- The heat sink (1542) is positioned on the semiconductor chip (1524a) with the solder bumps (1550b) aligned with a corresponding plurality of contacts as shown in Fig. 25;
- The solder bumps (1550a and 1550b) are sequentially reflowed; and
- The remaining space between the dielectric sheet (1512), the chip (1524a), and the heat sink (1542) is encapsulated with a flowable material (1534) that is subsequently cured.

These are limitations set forth in claims 11-14 of the applicant's invention.

However, Smith lacks a simultaneous solder reflow step, which is a limitation set forth in claim 11 of the applicant's invention. Ho et al. teach a simultaneous solder reflow step for joining a heat sink, a chip, and a substrate together (see column 4, lines 51-55).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the teachings of Smith by using the simultaneous solder reflow step as taught by Ho et al. in order to eliminate a second solder reflow step. Ho et al. recognize that eliminating process steps simplifies processing (see column 2, lines 33-36).

7. Claims 11, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (US 5,777,385 from applicant's IDS) in view of Ho et al. (US 6,507,104 B2).

Referring to Figs. 2-3 and column 3, line 11 to column 4, line 5, Wu discloses a semiconductor packaging method that includes the following features:

- A ceramic wiring substrate (14);
- An integrated circuit chip (13) with a plurality of solder bumps (29) on its active side;
- A silicon heat spreader (22) with a plurality of solder bumps (25) attached to one side;
- The integrated circuit chip (13) is positioned on the substrate (14), it being implied that the solder bumps (29) are aligned with pads corresponding to wiring traces in the substrate (14);
- The heat spreader (22) is positioned on the integrated circuit chip (13); and
- The solder bumps (29 and 25) are reflowed sequentially.

These are limitations set forth in claims 11, 15 of the applicant's invention.

However, Wu lacks a simultaneous solder reflow step, which is a limitation set forth in claim 11 of the applicant's invention. Ho et al. teach a simultaneous solder reflow step for joining a heat sink, a chip, and a substrate together (see column 4, lines 51-55).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the teachings of Wu by using the simultaneous solder reflow step as taught by Ho et al. in order to eliminate a second solder reflow

step. Ho et al. recognize that eliminating process steps simplifies processing (see column 2, lines 33-36).

Response to Arguments

8. Applicant's arguments (see page 5 of preliminary amendment filed on 16 October 2003) with respect to claims 11-15 have been considered but are moot in view of the new grounds of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot
Patent Examiner
Art Unit 2813